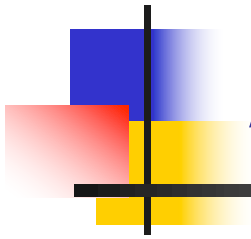

Chapter 8
Delay Fault Testing

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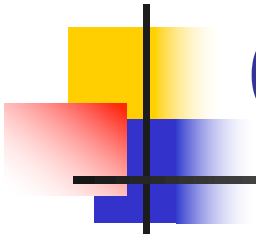
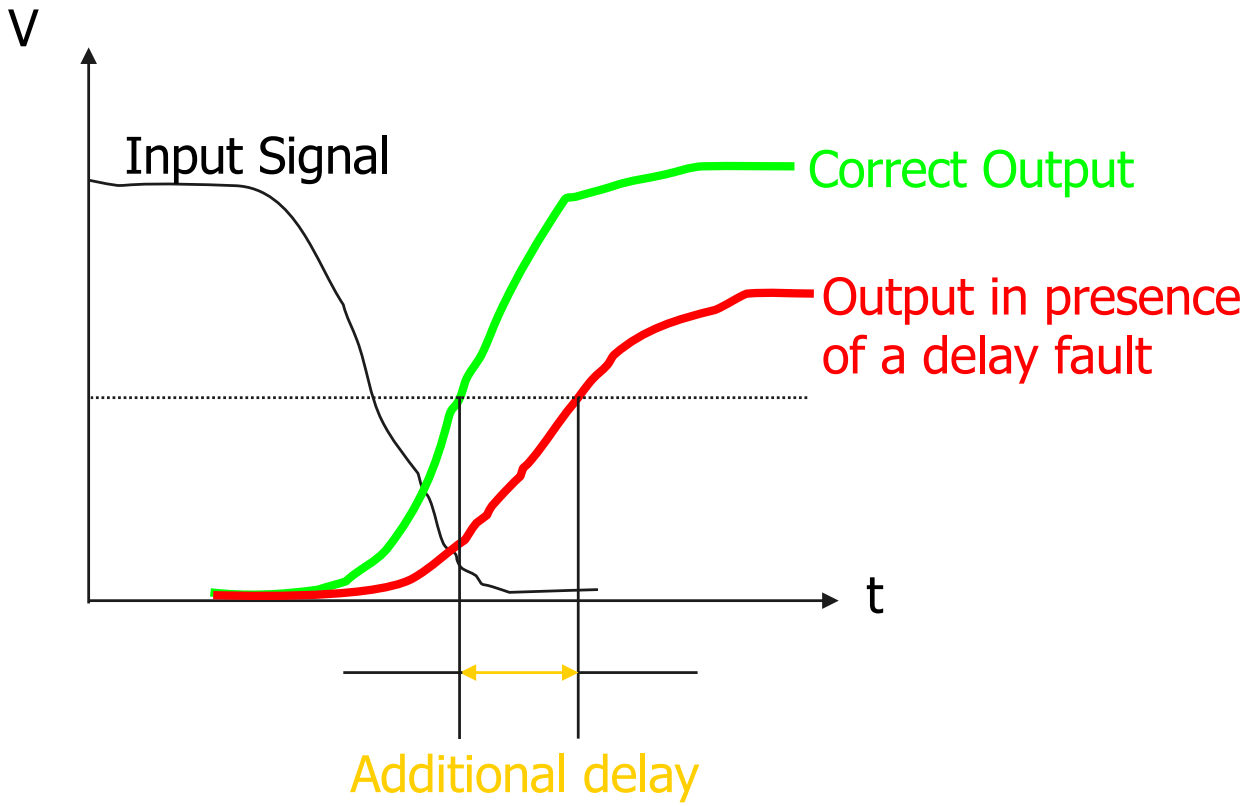


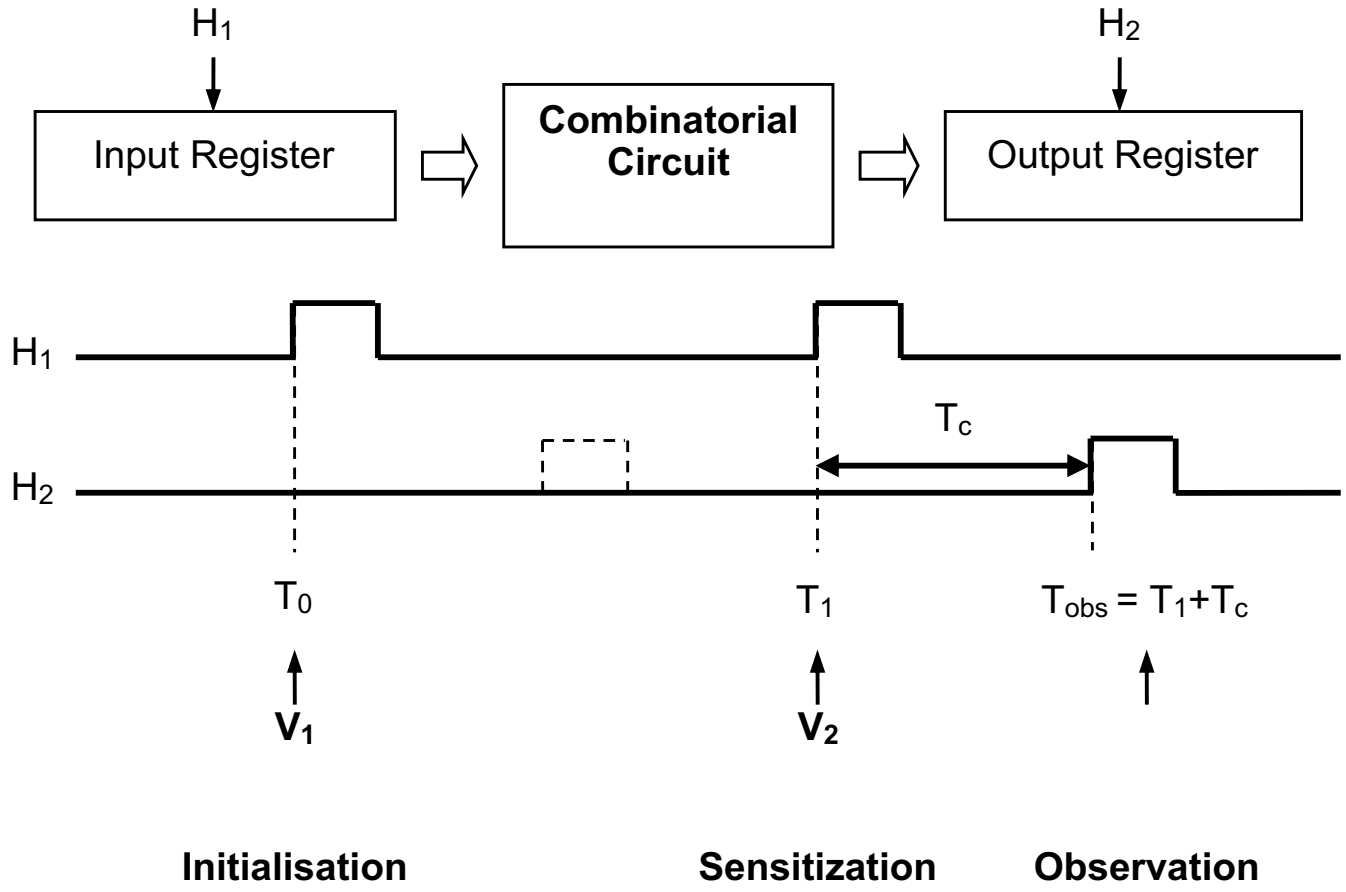
Outline

- Modelling
- Delay fault testing process
- Scan process for delay fault testing

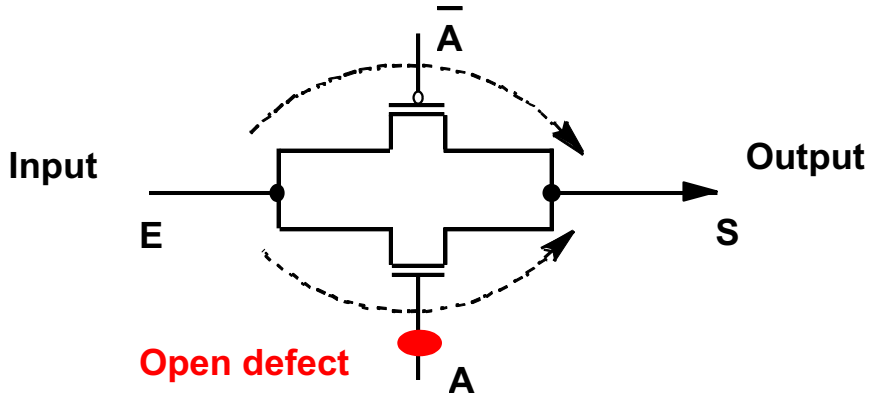
Delay Fault Principle

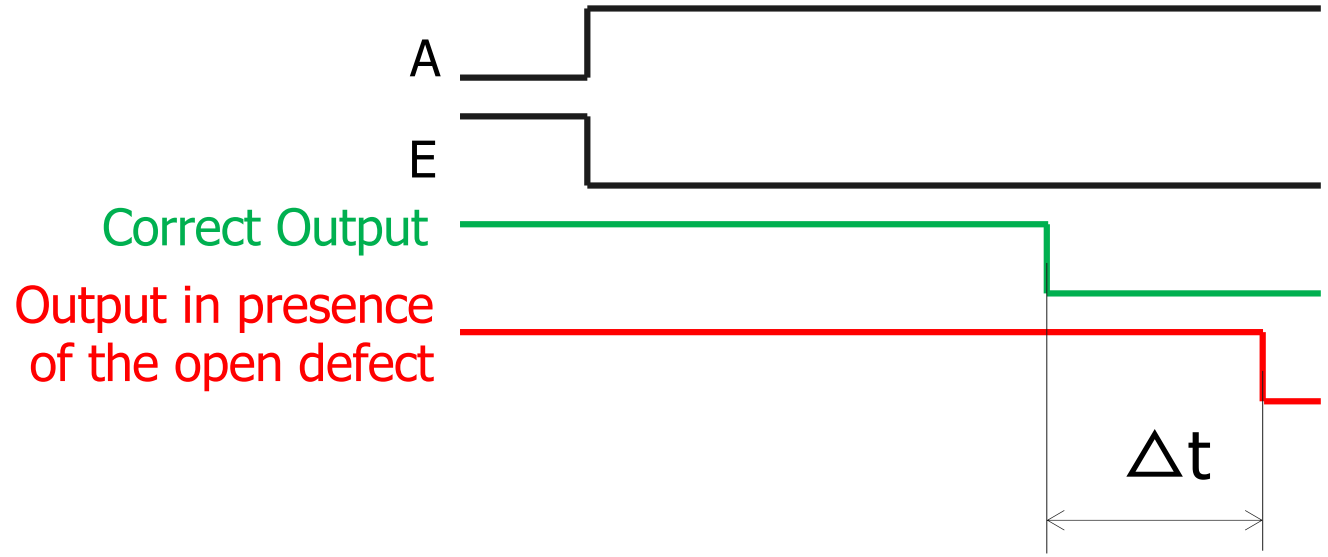


Delay Fault Testing Principle

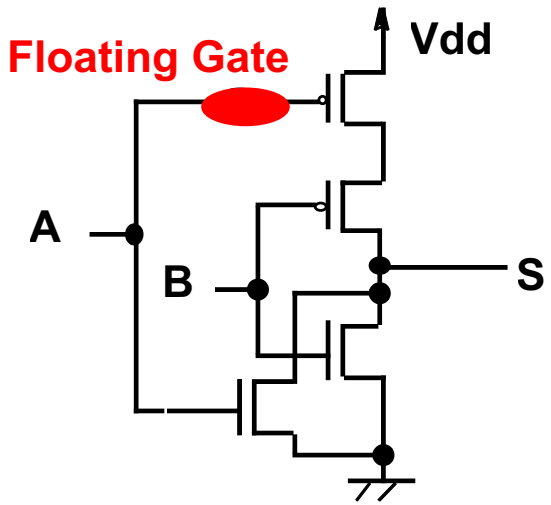


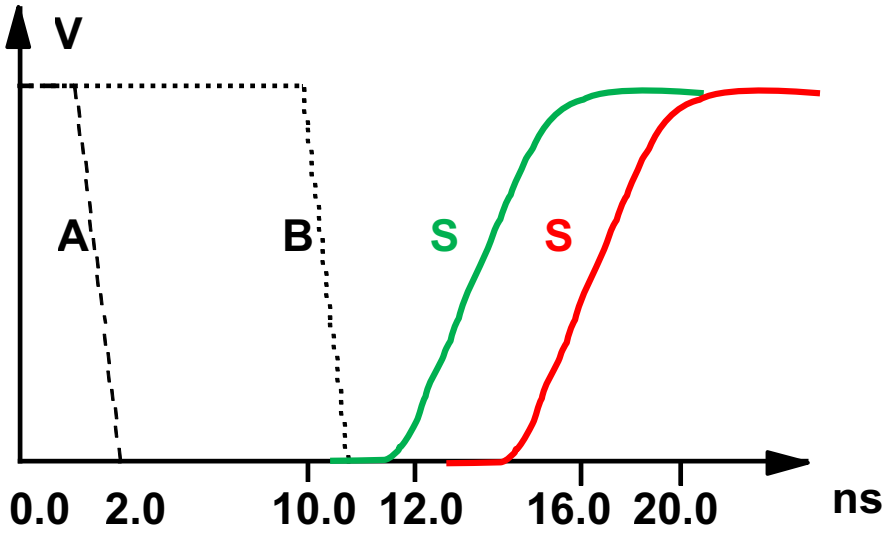
Physical Origins



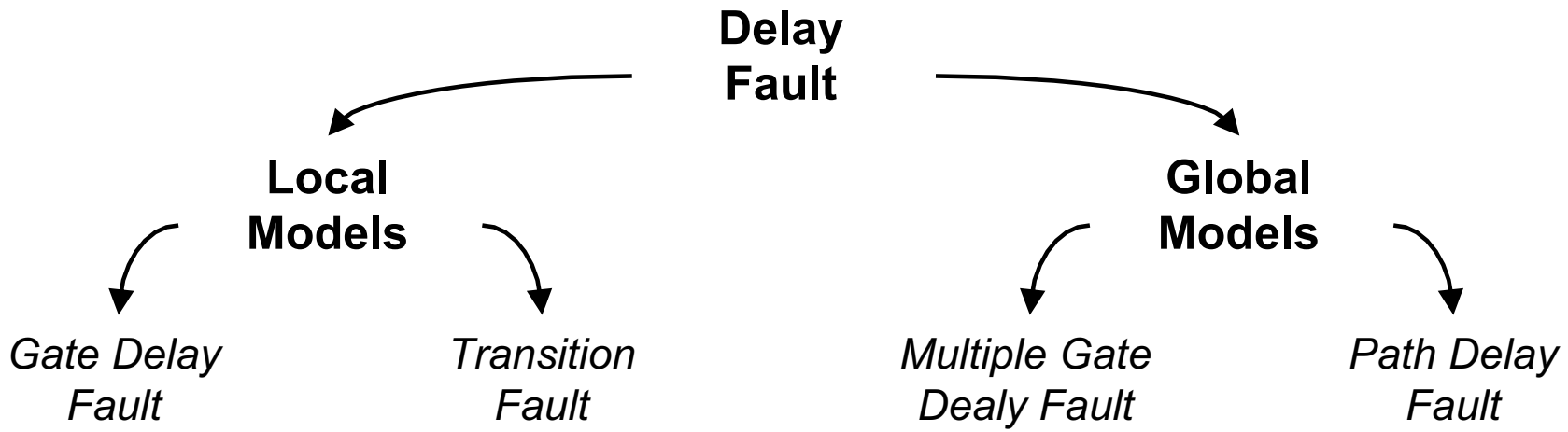


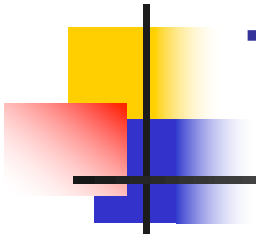
Physical Origins





Classification



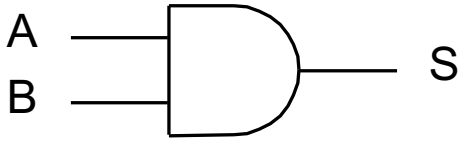


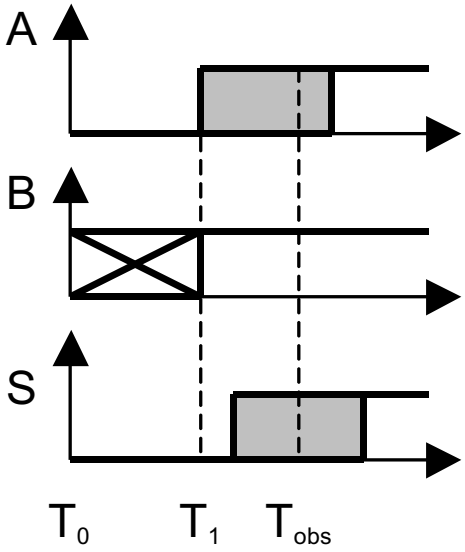
Transition Fault Definition

- The failure-induced delay is assumed to be long enough to cause an error regardless of the path used to propagate it
- The number of possible faults in the circuit remains limited to the number of connections of the circuit or even double if we consider the "slow-to-rise" and "slow-to-fall" faults
- The major drawback is that only the qualitative aspect of faults is taken into account, which limits its use to the particular case of large delay faults
- The transition fault model is very often used in industrial applications because it is simple to handle and, moreover, it is very close to the SAF model from a test vector generation point of view

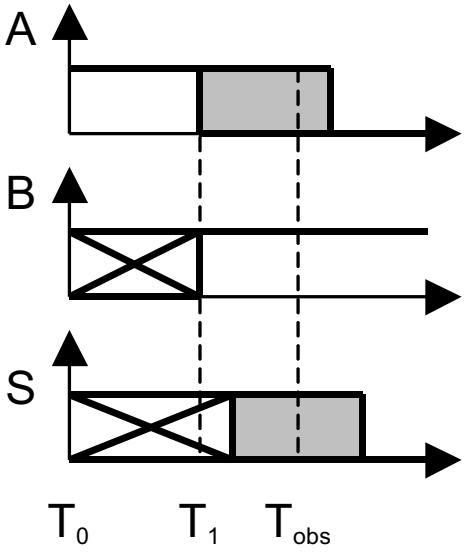
Transition Fault Example

- AND-gate example

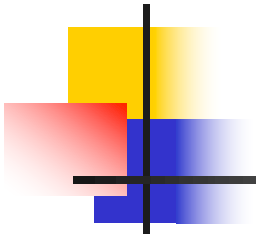




a) Slow-to-Rise on A



b) Slow-to-Fall on A



Path Delay Fault Definition

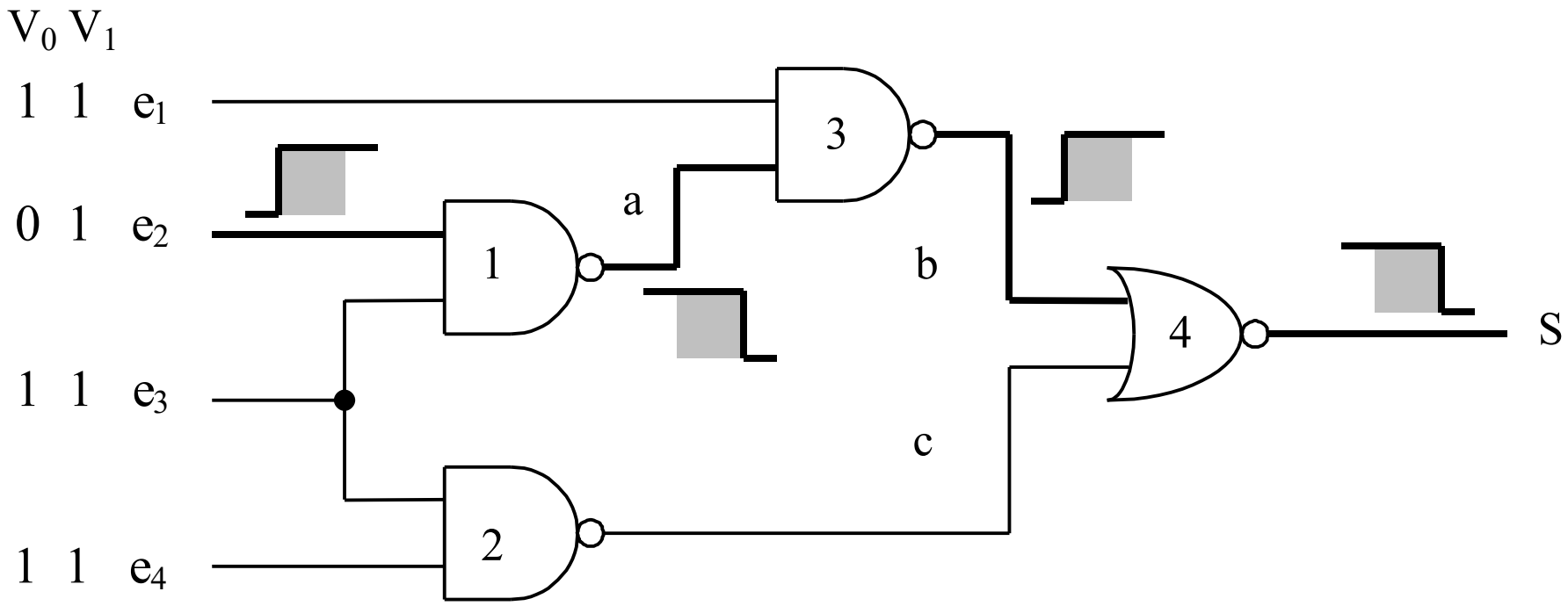
- The delay fault can be distributed over the entire path (taking into account non-local faults)
- The output response is observed at the nominal operating range of the DUT
- The path delay fault model is effective with faults of any size
- the presence of other faults does (theoretically) not affect the ability to test a given path. This therefore makes it possible to manage multiple faults.
- The path delay fault model is realistic and effective if **all paths** are tested

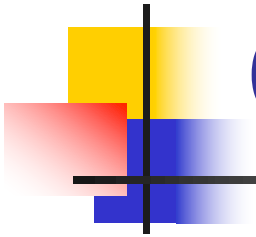
Path Delay Fault Issue

- The number of structural paths in a real circuit is usually large
- The number of functional paths is generally lower but remains significant
- Need to choose a smaller subset
- For example the longest structural paths
- **CAUTION** if there is a fault not sensitized by the chosen sub-assembly, it will never be detected

DUT	*# structural path*	*# structural longest path*
C432	83926	27
C499	9440	18
C880	8642	35
C1355	4173216	41
C1908	729057	48
C2670	679884	44
C3540	28676671	58
C5315	1341305	56
C6288	$>10^{20}$	218
C7552	726493	49

PDF Testing Example

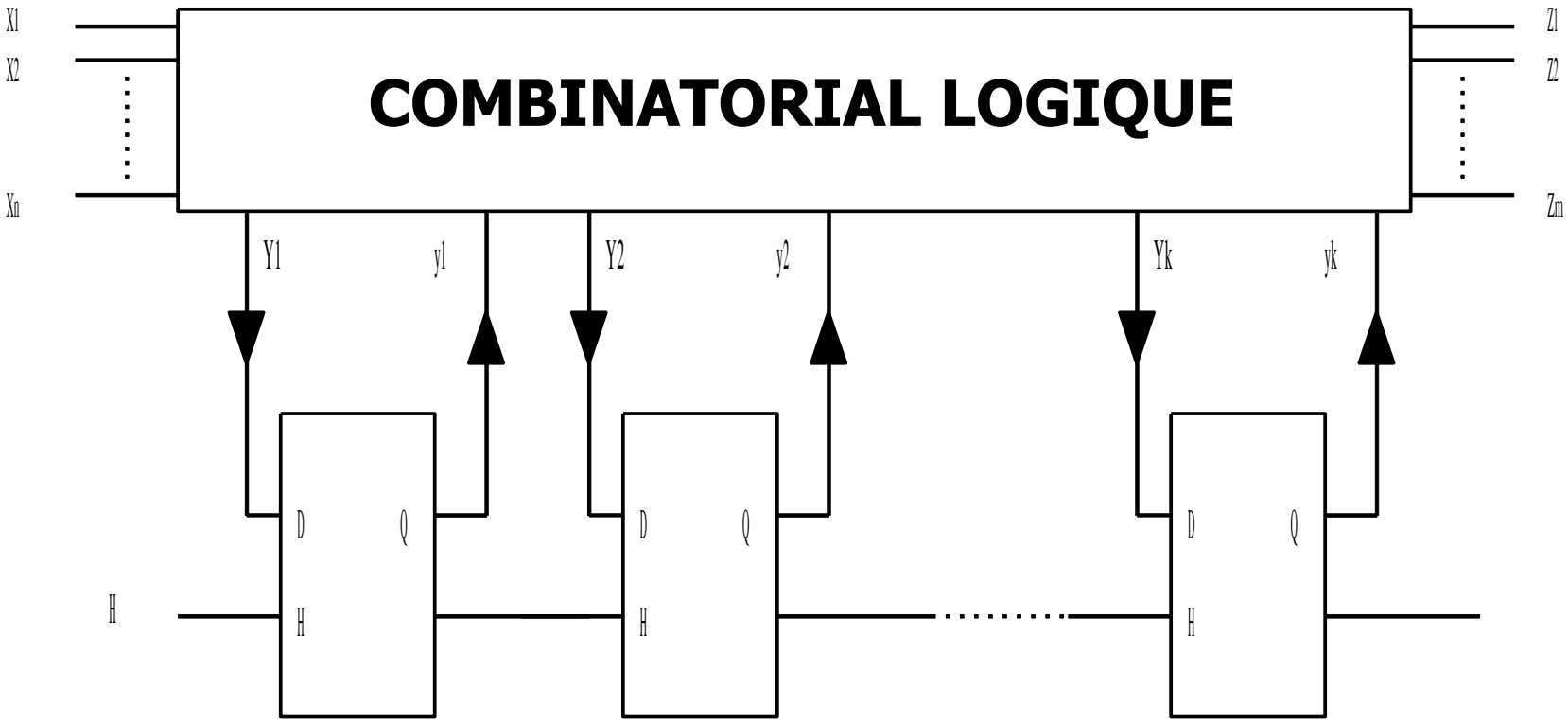




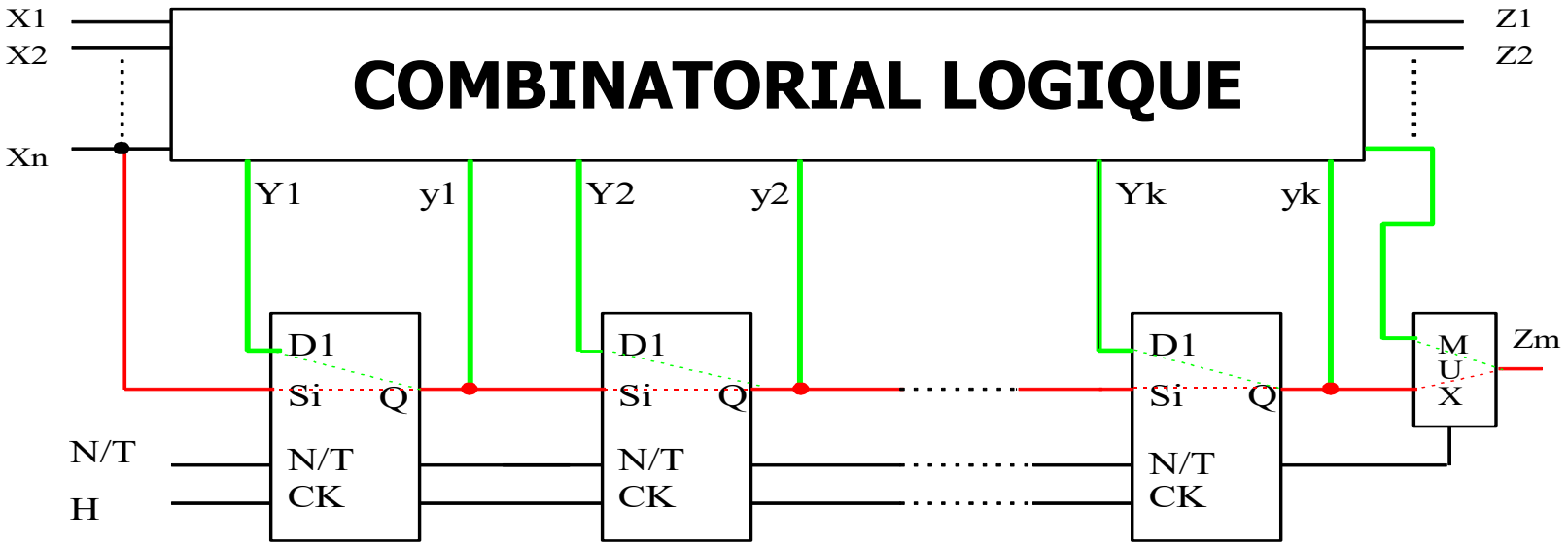
Outline

- Modelling
- Delay fault testing process
- **Scan process for delay fault testing**

Scan Path

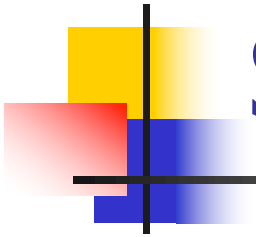

X1
X2
Xn
COMBINATORIAL LOGIQUE
Z1
Z2
Zm
Y1
y1
Y2
y2
Yk
yk
D
Q
H
D
Q
H
D
Q
H
H

Scan Path



Scan path

Functional path



Scan Test Process

0) Test of the scan chain (sequence of k times 01)

1) Place the circuit in test mode (N / T = 1)

2) Shift-in the test vector {y1, ..., yk} inside the scan path

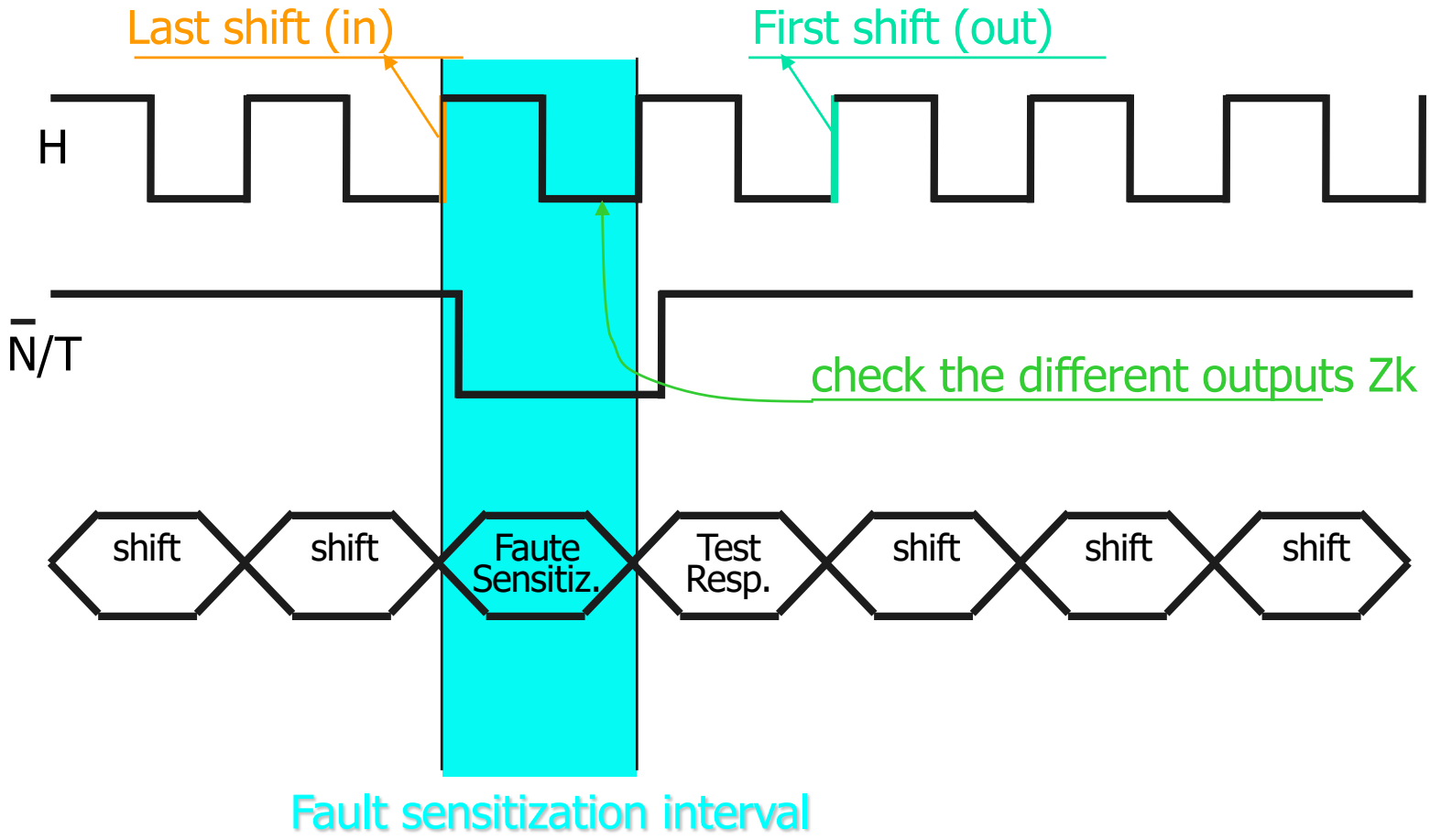
3) Set the corresponding test values on the primary inputs Xi

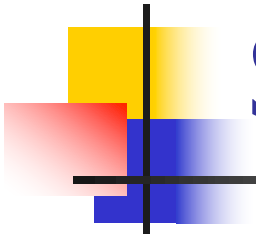
4) Place the circuit in functional mode (N / T = 0) and after a time necessary for the stabilization of the outputs of the combinatorial part, check the different outputs Zk

5) Apply a clock pulse to capture the test responses into the scan chain

6) Place the circuit in test mode (N / T = 1) and the contents of the shift register via the output Zm and compare it with the expected results (shift-in at the same time the next test vector)

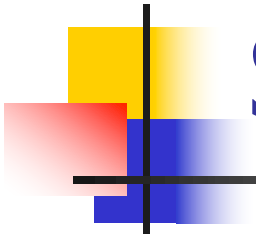
Scan Test Timing





Scan Test v.s. Delay Fault

- Issue
  - Application of a pair of vectors (V1, V2)
  - V1 and V2 are independents
- Solutions
  - Scan chain modification
  - Clock scheme modification



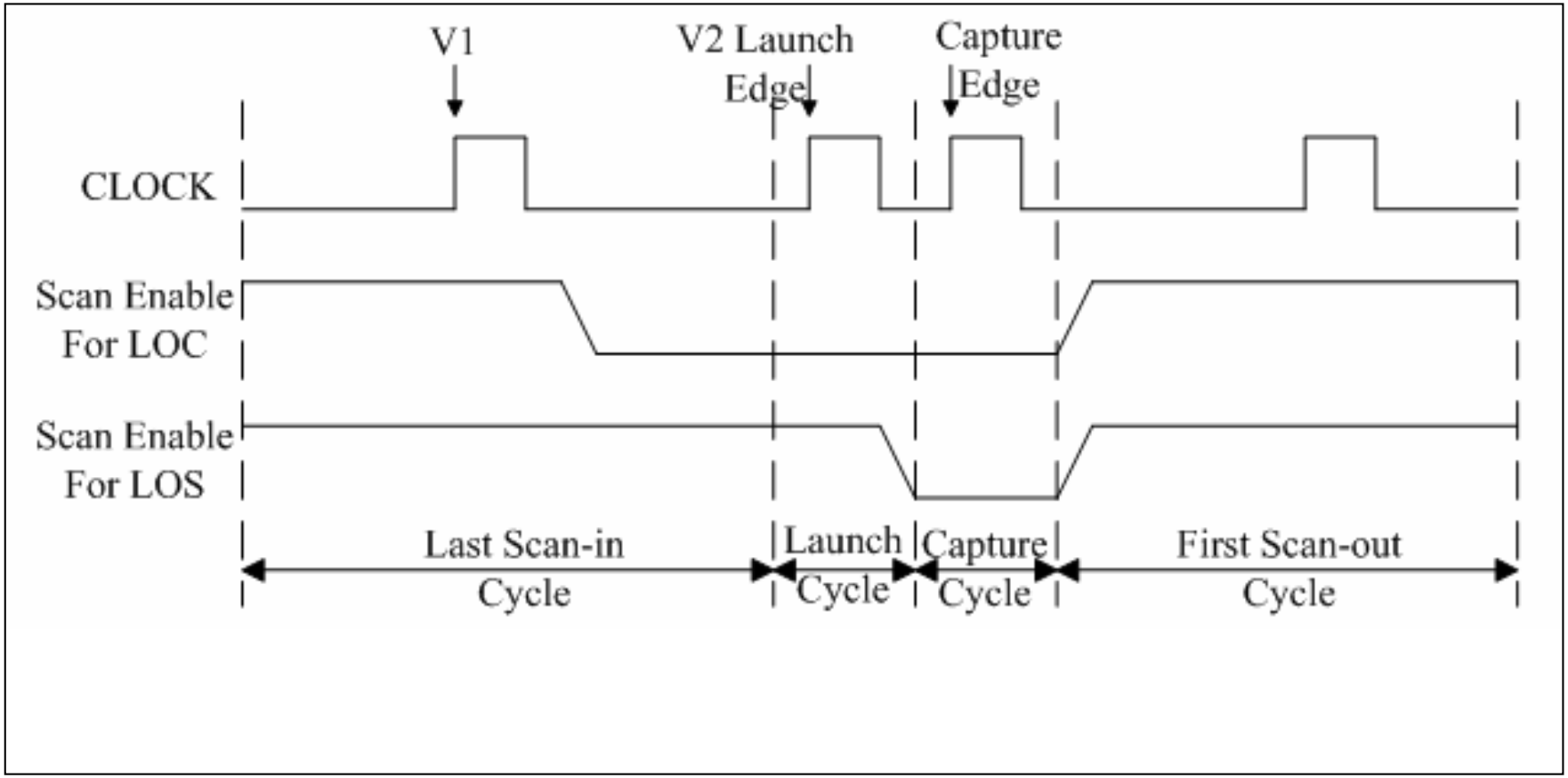
Scan Chain Modification

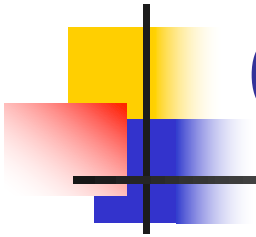
- Double the size of the scan chain
- Interleave V1 and V2 before loading
- Load the resulting vector
- A single shift allows to apply V2

Clock Scheme Modification

- LOC - Launch-Off-Capture
  - V1 → Vector loaded serially
  - V2 → DUT response of V1
- LOS – Launch-Off-Shift
  - V1 → Vector loaded serially
  - V2 → Obtained by one shift of V1

LOC / LOS Clock Schemes





Conclusion

- Transition fault testing
  - LOC → widely used
  - LOS → more effective
- Path delay fault testing
  - A set of critical path
  - A set of paths covering a maximum of paths